```
=> d his
     (FILE 'USPAT' ENTERED AT 10:26:28 ON 18 APR 1997)
L1         13861 S EPROM OR EEPROM
L2          6468 S L1 AND (READ? OR RETRIEV? OR SENS? OR DETERMIN?)(2A)DATA
L3            26 S L2 AND FLOAT?(3A)BITLINE
L4           110 S L2 AND FLOAT?(3A)(BIT OR COLUMN OR SENSE OR DIGIT)(2A)LI
NE
L5           131 S L3 OR L4
L6            31 S L5 AND (SENS? OR DETERMIN?)(3A)THRESHOLD
=> d l6 1-
```

1. 5,616,510, Apr. 1, 1997, Method for making multimedia storage system with highly compact memory cells; Chun C. D. Wong

2. 5,615,165, Mar. 25, 1997, Non-volatile semiconductor memory device and memory system using the same; Tomoharu Tanaka, et al., 365/230.06, 230.01 [IMAGE AVAILABLE]

3. 5,594,696, Jan. 14, 1997, Improvemetns in a detection circuit with a level shifting circuit; James A. Komarek, et al., 365/208; 327/52, 56 [IMAGE AVAILABLE]

4. 5,579,260, Nov. 26, 1996, Non-volatile semiconductor memory device and data programming method; Hiroshi Iwahashi, 365/185.24, 185.01, 189.05

5. 5,570,315, Oct. 29, 1996, Multi-state **EEPROM** having write-verify control circuit; Tomoharu Tanaka, et al., 365/185.22, 185.03, 185.12, 185.17, 185.18, 185.21 [IMAGE AVAILABLE]

6. 5,557,568, Sep. 17, 1996, Non-volatile semiconductor memory device with verify mode for verifying data written to memory cells; Junichi Miyamoto, et al., 365/185.22, 185.11, 185.17, 185.25 [IMAGE AVAILABLE]

7. 5,546,351, Aug. 13, 1996, Non-volatile semiconductor memory device and memory system using the same; Tomoharu Tanaka, et al., 365/230.06, 230.01 [IMAGE AVAILABLE]

8. 5,546,341, Aug. 13, 1996, Nonvolatile semiconductor memory; Kang D. Suh, et al., 365/185.33, 185.29, 218 [IMAGE AVAILABLE]

9. 5,541,879, Jul. 30, 1996, Nonvolatile semiconductor memory having program verifying circuit; Kang D. Suh, et al., 365/185.22, 185.05, 189.05, 201 [IMAGE AVAILABLE]

10. 5,537,362, Jul. 16, 1996, Low-voltage **EEPROM** using charge-pumped word lines; Manzur Gill, et al., 365/233.5, 189.11, 230.06 [IMAGE

AVAILABLE]

11. 5,521,865, May 28, 1996, Non-volatile semiconductor memory device for storing multi-value data; Kazunori Ohuchi, et al., 365/185.22, 185.03, 185.21, 205 [IMAGE AVAILABLE]

12. 5,517,138, May 14, 1996, Dual row selection using multiplexed tri-level decoder; Robert L. Baltar, et al., 326/105, 10, 106; 365/200, 230.06 [IMAGE AVAILABLE]

13. 5,473,563, Dec. 5, 1995, Nonvolatile semiconductor memory; Kang D. Suh, et al., 365/185.13, 189.01, 189.05, 230.06 [IMAGE AVAILABLE]

14. 5,467,300, Nov. 14, 1995, Grounded memory core for Roms, **Eproms**, and EEpproms having an address decoder, and sense amplifier; James A. Komarek, et al., 365/185.16, 94, 185.21, 185.25, 203 [IMAGE AVAILABLE]

15. 5,465,236, Nov. 7, 1995, Nonvolatile semiconductor memory system with a plurality of erase blocks; Kiyomi Naruke, 365/185.11, 185.18, 185.26, 185.33, 222 [IMAGE AVAILABLE]

16. 5,452,249, Sep. 19, 1995, Non-volatile semiconductor memory device with verify mode for verifying data written to memory cells; Junichi Miyamoto, et al., 365/185.13, 185.24, 189.01, 189.11 [IMAGE AVAILABLE]

17. 5,422,846, Jun. 6, 1995, Nonvolatile memory having overerase protection; Kuo-Tung Chang, et al., 365/185.12, 51, 63, 218 [IMAGE AVAILABLE]

18. 5,408,431, Apr. 18, 1995, Single transistor **EEPROM** architecture; Nagesh Challa, 365/185.17, 185.18, 185.26, 185.28, 189.04 [IMAGE AVAILABLE]

19. 5,386,132, Jan. 31, 1995, Multimedia storage system with highly compact memory device; Chun C. D. Wong, 257/316, 320; 365/185.26, 185.29 [IMAGE AVAILABLE]

20. 5,377,147, Dec. 27, 1994, Method and circuitry for preconditioning shorted rows in a nonvolatile semiconductor memory incorporating row redundancy; Amit Merchant, et al., 365/185.09, 185.12, 185.21, 185.22, 185.24, 185.33, 203, 210, 218; 371/10.3 [IMAGE AVAILABLE]

21. 5,375,094, Dec. 20, 1994, Nonvolatile semiconductor memory system with a plurality of erase blocks; Kiyomi Naruke, 365/222, 185.11, 218, 230.03 [IMAGE AVAILABLE]

22. 5,361,227, Nov. 1, 1994, Non-volatile semiconductor memory device

and memory system using the same; Tomoharu Tanaka, et al., 365/185.22, 185.08, 185.17, 185.27, 200, 201 [IMAGE AVAILABLE]

23. 5,357,465, Oct. 18, 1994, Single transistor **EEPROM** memory cell; Nagesh Challa, 365/185.18, 149, 182, 185.12, 185.23, 185.26, 185.27, 185.33 [IMAGE AVAILABLE]

24. 5,347,489, Sep. 13, 1994, Method and circuitry for preconditioning shorted rows in a nonvolatile semiconductor memory incorporating row redundancy; Amit Merchant, et al., 365/203, 185.2, 185.24, 200, 210, 218, 230.06; 371/10.3 [IMAGE AVAILABLE]

25. 5,345,418, Sep. 6, 1994, Single transistor **EEPROM** architecture; Nagesh Challa, 365/185.17, 51, 185.18, 185.26, 185.3, 185.33, 218, 226 [IMAGE AVAILABLE]

26. 5,327,383, Jul. 5, 1994, Method and circuitry for erasing a nonvolatile semiconductor memory incorporating row redundancy; Amit Merchant, et al., 365/185.24, 184, 185.09, 185.12, 185.21, 185.22, 185.33, 200, 201, 210 [IMAGE AVAILABLE]

27. 5,287,315, Feb. 15, 1994, Skewed reference to improve ones and zeros in **EPROM** arrays; John F. Schreck, et al., 365/185.21, 185.11, 185.16, 189.09 [IMAGE AVAILABLE]

28. 5,197,027, Mar. 23, 1993, Single transistor **EEPROM** architecture; Nagesh Challa, 365/185.16, 51, 185.13, 185.18, 185.26, 185.3, 185.33, 218 [IMAGE AVAILABLE]

29. 5,117,394, May 26, 1992, High speed differential sense amplifier for use with single transistor memory cells; Alaaeldin A. M. Amin, et al., 365/185.21, 185.25, 202, 208, 210 [IMAGE AVAILABLE]

30. 4,916,640, Apr. 10, 1990, Video image processing system; Michael L. Gasperi, et al., 382/291, 271 [IMAGE AVAILABLE]

31. 4,715,014, Dec. 22, 1987, Modified three transistor **EEPROM** cell; James A. Tuvell, et al., 365/185.28, 185.1, 185.25, 187 [IMAGE AVAILABLE]